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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,685	10/03/2003	Darin J. Douma	15436.250.24.1	9973

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EXAMINER	
FILE, ERIN M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,685	DOUMA ET AL.	
	Examiner	Art Unit	
	Erin M. File	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/3/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/9/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 2004/0179138).

Claim 14, Wang discloses:

- receiving an asserted synchronization signal from a phase locked loop, the phase locked loop disposed on the controller chip (abstract, lines 5-6, 9-11, 12-15);
- determining whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency (abstract, lines 5-6, 9-11, 12-15, [0053])
- asserting a lock signal if the phase locked loop has locked onto a data signal ([0051]-[0053], the synchronization signal from the synchronization phase locked

loop is asserted if the valid channel frequency is held for a predetermined time, T_p).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 9, 10, and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) in view of Van Roon (NPL) .

Claims 1, 9, Wang discloses:

- a controller chip that includes a phase locked loop adapted to operate in a hunting mode and a locked mode (abstract, lines 2-4 describes search, or hunting, mode, abstract, lines 6-11 describe locked mode)
- the phase locked loop asserts a synchronization signal in the hunting mode when a hunting frequency passes through a data signal frequency (abstract, lines 5-6, 9-11, 12-15)
- the phase locked loop keeps the synchronization signal asserted as long as the phase locked loop is locked onto a data signal ([0053]);
- produces a lock signal if the synchronization signal is asserted for a least a specified period of time ([0051]-[0053], the synchronization signal from the

synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, T_p).

Wang fails to disclose and a timing circuit that measures a period of time, T_p, that the synchronization signal is asserted, however, Van Roon discloses a simple timer for timing a signal (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

Claim 2, Wang fails to disclose a timing circuit which is an analog timer comprising a capacitor and a resistor network. However, an analog timer which includes a capacitor and a resistor network is extremely well known in the art. Van Roon discloses a analog timer with a capacitor and resistor network (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

Claim 3, although Wang fails to disclose the timing circuit comprises a transistor for resetting the timing circuit, Van Roon discloses a transistor for resetting the circuit (p. 3, 4-2, pin 4 is reset by transistor Q25). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

Claim 10, Wang further discloses the translation circuit comprising a timer that measures a period of time that the synchronization signal is asserted ([0051]-[0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, T_p).

Claim 15, Wang further discloses determining that the synchronization signal is caused by the phase locked loop locking onto the data signal if the period of time that the synchronization signal is asserted is greater than a specified period of time ([0051]-[0053], the synchronization signal from the synchronization phase locked loop is asserted if the valid channel frequency is held for a predetermined time, T_p);

Wang fails to disclose measuring a period of time that the synchronization signal is asserted, T_p, however, Van Roon discloses a simple timer for timing a signal (p. 2, fig. 3). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

5. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) and Van Roon as applied to claim 3 above, and further in view of Transistors Non-Patent Literature.

Claim 4, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well

known in the art as low cost transistor with low power consumption at low voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Wang.

Claim 5, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is a field effect transistor (p. 3, FET's as Transistors). Because FET transistor are well known in the art as low cost transistor which can operate at high voltage levels, it would have been obvious to one skilled in the art at the time of invention to incorporate a FET transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Wang.

6. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) as applied to claim 14 above, and further in view of Lee (U.S. Patent No. 5,886,748).

Claim 16, although Wang fails to disclose an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

Claim 17, although Wang fails to disclose comparing the lock signal with a reference signal to produce the lock signal, Lee discloses comparing the lock signal with a reference signal to produce the lock signal (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

7. Claim 6, 7, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) and Van Roon (NPL) as applied to claim 2 above, and further in view of Lee (U.S. Patent No. 5,886,748).

Claims 6, 11, 12, neither Wang nor Van Roon disclose an input level detector that compares the synchronization signal with a reference signal and produces logical signals that may be fed into the timing circuit, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

Claim 7, neither Wang nor Van Roon disclose a comparator that receives a signal from the capacitor and resistor network and a reference signal as input and that outputs the lock signal to the host device based on the value of the reference signal compared to the signal from the capacitor and resistor network, Lee discloses comparing the a timing

signal such as that which comes from the capacitive resistive network as disclosed by Van Roon with a reference signal and producing logical timing signals (col. 2, lines 51-55). Because this signal allows for more effective and accurate synchronization of the signal, it would be obvious to one skilled in the art at the time of invention to incorporate the comparator as disclosed by Lee into the invention of Wang.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138), Van Roon (NPL), and Lee (U.S. Patent No. 5,886,748) as applied to claim 7 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

Claim 8, neither Wang, nor Van Roon, nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Wang, Van Roon and Lee.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138), Van Roon (NPL), and Lee (U.S. Patent No. 5,886,748) as applied to claim 12 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

Claim 13, neither Wang nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Wang and Lee.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (U.S. Pub. No. 2004/0179138) as applied to claim 14 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

Claim 18, Wang fails to disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal

changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the invention of Wang.

11. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,886,748) in view of Van Roon (NPL).

Claim 19, Lee discloses

- a comparator circuit that compares the output signal with a reference signal such that a lock signal is asserted based on the comparison of the output signal with the reference signal. (col. 2, lines 51-55)

Lee fails to disclose:

- a timing circuit that measures a period of time that a signal is asserted
- the timing circuit uses a capacitor
- wherein the timing circuit generates an output signal having a voltage across the capacitor

However, Van Roon discloses:

- a timing circuit that measures a period of time that a signal is asserted (fig. 2, 3)
- the timing circuit uses a capacitor (p. 2, fig. 3)
- wherein the timing circuit generates an output signal having a voltage across the capacitor (see pin 3 output of fig. 4-2)

Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Wang.

Claim 20, although Lee fails to disclose the timing circuit comprises a transistor for resetting the timing circuit, Van Roon discloses a transistor for resetting the circuit (p. 3, 4-2, pin 4 is reset by transistor Q25). Because the 555 timer as disclosed by Van Roon offers the advantages of being an inexpensive, stable, and user friendly integrated circuit (p. 1, line 2), it would have been obvious to one skilled in the art at the time of invention to use the timer as disclosed by Van Roon in the invention of Lee.

12. Claim 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,886,748) and Van Roon (NPL) as applied to claim 20 above, and further in view of Transistors Non-Patent Literature.

Claim 21, Van Roon fails to disclose the type of transistors used in his timer, however, Transistors Non-Patent Literature discloses transistor is at least one of a PNP and NPN bipolar junction transistor (p. 3, The NPN Transistor). Because NPN transistor are well known in the art as low cost transistor with low power consumption at low voltage levels,

it would have been obvious to one skilled in the art at the time of invention to incorporate a NPN transistor as disclosed by Transistors Non-Patent Literature into the combined invention disclosed by Van Roon and Lee.

13. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. Patent No. 5,886,748) and Van Roon (NPL) as applied to claim 19 above, and further in view of IBM Technical Disclosure Bulletin, May 1990.

Claims 22, 23, neither Lee nor Van Roon, nor Lee disclose a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value. However, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator includes feedback that changes a logical level of the lock signal output to the host device when the value of the lock signal changes by some value greater than a hysteresis threshold value (see part 3 and figure 2). The disclosure further states that this scheme has the advantage of providing a stabilized synchronization acquisition (part 3, lines 2-3). Because of this advantage it would have been obvious to one skilled in the art a the time of invention to incorporate the phase lock as disclosed by the IBM Technical Disclosure Bulletin, May 1990 into the combined invention of Van Roon and Lee.

Claim 24, Lee discloses comparing the synchronization signal with a reference signal and producing logical signals that may be fed into the timing circuit (col. 2, lines 51-55).

Claim 25, IBM Technical Disclosure Bulletin, May 1990 discloses a comparator circuit asserts a lock signal when the voltage across the capacitor exceeds the reference signal (see part 3 and figure 2). The combined invention of Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 does not disclose expressly the capacitor charges slowly and discharges quickly. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a capacitor which charges slowly and discharges quickly. Applicant has not disclosed that the capacitor charges slowly and discharges quickly provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990. Therefore, it would have been obvious to one of ordinary skill in this art to modify Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 to obtain the invention as specified in claim 25.

Claim 26, IBM Technical Disclosure Bulletin, May 1990 discloses comparator asserts a lock signal when the reference signal exceeds the voltage across the capacitor see part 3 and figure 2). The combined invention of Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 does not disclose expressly the capacitor charges slowly and discharges quickly. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use a capacitor which charges quickly and discharges slowly. Applicant has not disclosed that the capacitor charges quickly and discharges slowly provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have

expected Applicant's invention to perform equally well with Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990. Therefore, it would have been obvious to one of ordinary skill in this art to modify Lee, Van Roon, and the IBM Technical Disclosure Bulletin, May 1990 to obtain the invention as specified in claim 25.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 6, 11, and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following claims contain language which is inexact and makes the intention of the claimed subject matter unclear:

Claim 6, "may be fed into the timing circuit".

In Claim 11, "and when the synchronization signal is asserted because a hunting frequency passes through a data signal frequency in hunting mode".

In Claim 17, "with a reference signal to produce the lock signal useful by a host device coupled to the fiber-optic transponder".

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin M. File whose telephone number is (571)272-6040. The examiner can normally be reached on M-F 1:00PM-9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Erin M. File

12/10/2006

MOHAMMED GHAYOUR
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